Amendments to the Claims

The listing of claims below will replace all prior versions and listings of claims in the present application.

Claim Listing

| 1 | 1. (Original) A method of verifying correct operation of a forward error |
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| 2 | correction decoder, comprising the steps of: |
| 3 | programmably selecting a desired number of errors for insertion into a plurality of |
| 4 | data signals; |
| 5 | defining a plurality of code words of the data signals; |
| 6 | inserting into one of the data signals the desired number of errors using an error |
| 7 | insertion circuit; |
| 8 | repeating said inserting step in an iterative fashion to insert into different data |
| 9 | signals the desired number of errors wherein the errors are placed within |
| 10 | the code words of the data signals at different location permutations for |
| 11 | each data signal; |
| 12 | transmitting the data signals with the inserted errors to a receiver; and |
| 13 | determining that the data signals received at the receiver contain the inserted |
| 14 | errors. |
| 1 | 2. (Original) The method of Claim 1 wherein said repeating step cycles through |
| 2 | all possible permutations of all the code word locations. |
| 1 | 3. (Original) The method of Claim 1 wherein the error insertion circuit operates |
| 2 | in one of a plurality of modes, including a short frame mode for shorter permutation |
| 3 | cycles, and further comprising the steps of: |
| 4 | selecting the short frame mode for operation; and |
| 5 | in response to said selecting step, limiting said repeating step to cycle through less |
| 6 | than all possible permutations of all the code word locations. |

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| 1 | 4. (Original) The method of Claim I wherein: |
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| 2 | the data signal is a SONET data signal having nine rows; and |
| 3 | said repeating step results in the insertion of errors in 32 code words defined |
| 4 | within each of the nine SONET rows. |
| | |
| 1 | 5. (Original) The method of Claim 1 wherein said repeating step stops after one |
| 2 | permutation cycle in response to the further step of programming the error insertion |
| 3 | circuit for single cycle operation. |
| 1 | 6 (Original) The method of Claim 1 wherein said determining stem includes the |
| 1 | 6. (Original) The method of Claim 1 wherein said determining step includes the step of examining an error accumulator count in the receiver to match a number of |
| 2 | |
| 3 | accumulated errors with the number of inserted errors. |
| 1 | 7. (Original) The method of Claim 6 wherein said examining step matches the |
| 2 | number of accumulated errors with the number of inserted errors using a modulo |
| 3 | function. |
| | |
| 1 | 8. (Original) The method of Claim 1 wherein: |
| 2 | the error insertion circuit includes an error mask for selectively preventing |
| 3 | insertion of one or more of the errors; and |
| 4 | said repeating step is limited to inserting errors in selected code words based on |
| 5 | the error mask. |
| 1 | 9. (Original) The method of Claim 1 wherein said repeating step includes the step |
| 2 | of tracking the location of a current code word in which an error is being inserted. |
| _ | of maxing the focusion of a current code word in which an error is come morrous. |
| 1 | 10. (Original) The method of Claim 9 wherein said tracking step includes the step |
| 2 | of incrementing one or more registers in a location counter having at least first, second, |
| 3 | and third registers, the first register corresponding to a column location, the second |
| 4 | register corresponding to an index location, and the third register corresponding to a byte |
| 5 | location. |

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| I | 11. (Original) A method of injecting a plurality of errors into a SONE 1 data |
|----|---|
| 2 | stream, comprising the steps of: |
| 3 | programming an error insertion circuit to select a desired number of errors for |
| 4 | insertion into a plurality of successive SONET data signals each having a |
| 5 | plurality of rows; |
| 6 | defining a plurality of forward error correction (FEC) code words within each of |
| 7 | the rows of the SONET data signals; |
| 8 | inserting the desired number of errors into a first one of the SONET data signals |
| 9 | at a first code word permutation location, using the error insertion circuit; |
| 10 | tracking the first code word permutation location in response to said step of |
| 11 | inserting the desired number of errors into the first SONET data signal; |
| 12 | and |
| 13 | inserting the desired number of errors into a second one of the SONET data |
| 14 | signals at a second code word permutation location, using the error |
| 15 | insertion circuit, and in response to said tracking step. |
| 1 | 12. (Original) The method of Claim 11 further comprising the step of |
| 2 | programming the error insertion circuit for single cycle operation. |
| 1 | 13. (Original) The method of Claim 11 further comprising the step of |
| 2 | programming the error insertion circuit for short frame mode operation. |
| 1 | 14. (Original) The method of Claim 11 wherein said tracking step includes the |
| 2 | step of incrementing one or more registers in a location counter having at least first, |
| 3 | second, and third registers, the first register corresponding to a SONET column location, |
| 4 | the second register corresponding to an index location, and the third register |
| 5 | corresponding to a byte location, the index and byte locations together representing a |
| 6 | SONET byte location. |
| 1 | 15. (Original) The method of Claim 11 wherein said inserting steps occur after |
| 2 | the further step of scrambling the SONET data signals. |

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| 1 | 16. (Original) An error injection circuit comprising: |
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| 2 | means for selectively programming a desired number of errors for insertion into a |
| 3 | plurality of data signals; |
| 4 | means for defining a plurality of code words of the data signals; and |
| 5 | means for repeatedly inserting the desired number of errors into different ones of |
| 6 | the data signals at different code word permutation locations. |
| 1 | 17. (Original) The error injection circuit of Claim 16 wherein said inserting |
| 2 | means cycles through all possible permutations of all the code word locations. |
| 1 | 18. (Original) The error injection circuit of Claim 16 further comprising means |
| 2 | for selecting a short frame mode of operation, wherein said inserting means limits |
| 3 | insertion of the errors to cycle through less than all possible permutations of all the code |
| 4 | word locations when the short frame mode of operation is selected. |
| 1 | 19. (Original) The error injection circuit of Claim 16 wherein: |
| 2 | the data signal is a SONET data signal having nine rows; and |
| 3 | said inserting means inserts errors in 32 code words defined within each of the |
| 4 | nine SONET rows. |
| 1 | 20. (Original) The error injection circuit of Claim 16 further comprising means |
| 2 | for selecting single cycle operation, wherein said inserting means stops inserting errors |
| 3 | after one permutation cycle when the single cycle operation is selected. |
| 1 | 21. (Original) The error injection circuit of Claim 16 further comprising error |
| 2 | mask means for selectively preventing insertion of one or more of the errors, wherein |
| 3 | said inserting means inserts errors in selected code words based on said error mask |
| 4 | means. |

| 1 | 22. (Original) The error injection circuit of Claim 16 wherein said insertion |
|----|---|
| 2 | means includes means for tracking the location of a current code word in which an error |
| 3 | is being inserted. |
| | |
| 1 | 23. (Original) The error injection circuit of Claim 16 wherein said tracking means |
| 2 | increments one or more registers in a location counter having at least first, second, and |
| 3 | third registers, the first register corresponding to a column location, the second register |
| 4 | corresponding to an index location, and the third register corresponding to a byte |
| 5 | location. |
| | |
| 1 | 24. (Cancelled) |
| 4 | |
| 1 | 25. (Currently Amended) The OC-192 input/output card of Claim 24-wherein |
| 2 | said verifying means includes: An OC-192 input/output card comprising: |
| 3 | four OC-48 processors; and |
| 4 | an OC-192 front-end application-specific integrated circuit (ASIC) connected to |
| 5 | said four OC-48 processors, said OC-192 front-end ASIC including |
| 6 | a transmitter having means for interleaving four OC-48 signals to create |
| 7 | an OC-192 signal, and means for encoding forward error |
| 8 | correction (FEC) codes in each of the four OC-48 signals, |
| 9 | a receiver having means for de-interleaving an OC-192 signal to create |
| 10 | four OC-48 signals, and means for decoding FEC codes in the OC- |
| 11 | 192 signal, and |
| 12 | means for verifying correct operation of said encoding means and said |
| 13 | decoding means, wherein said verifying means includes: |
| 14 | means for selectively programming a desired number of errors for |
| 15 | insertion into a plurality of successive SONET data signals; |
| 16 | means for defining a plurality of FEC code words of the SONET |

data signals;

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| 8 | means for repeatedly inserting the desired number of errors into |
|----|--|
| 9 | different ones of the SONET data signals at different code |
| 20 | word permutation locations; |
| 21 | means for routing the SONET data signals with the inserted errors |
| 22 | from said transmitter to said receiver; and |
| 23 | means for determining that the SONET data signals received at |
| 24 | said receiver contain the inserted errors. |
| 1 | 26. (Original) The OC-192 input/output card of Claim 25 wherein said inserting |
| 2 | means cycles through all possible permutations of all the FEC code word locations. |
| 1 | 27. (Original) The OC-192 input/output card of Claim 25 further comprising |
| 2 | means for selecting a short frame mode of operation, wherein said inserting means limits |
| 3 | insertion of the errors to cycle through less than all possible permutations of all the code |
| 4 | word locations when the short frame mode of operation is selected. |
| 1 | 28. (Original) The OC-192 input/output card of Claim 25 further comprising |
| 2 | means for selecting single cycle operation, wherein said inserting means stops inserting |
| 3 | errors after one permutation cycle when the single cycle operation is selected. |
| 1 | 29. (Original) The OC-192 input/output card of Claim 25 further comprising |
| 2 | error mask means for selectively preventing insertion of one or more of the errors, |
| 3 | wherein said inserting means inserts errors in selected code words based on said error |
| 4 | mask means. |
| 1 | 30. (Original) The OC-192 input/output card of Claim 25 wherein said insertion |
| 2 | means includes means for tracking the location of a current code word in which an error |
| 3 | is being inserted. |
| 1 | 31. (Currently Amended) The OC-192 input/output card of Claim 24 25 wherein |
| 2 | said programming means allows from one to four errors to be inserted in a given SONET |
| 3 | data signal. |

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| 1 | 32. (Currently Amended) An OC-192 input/output card comprising: |
|----|---|
| 2 | four OC-48 processors; and |
| 3 | an OC-192 front-end application-specific integrated circuit (ASIC) connected to |
| 4 | said four OC-48 processors, said OC-192 front-end ASIC including |
| 5 | a transmitter having means for interleaving four OC-48 signals to create |
| 6 | an OC-192 signal, and means for encoding forward error |
| 7 | correction (FEC) codes in each of the four OC-48 signals, |
| 8 | a receiver having means for de-interleaving an OC-192 signal to create |
| 9 | four OC-48 signals, and means for decoding FEC codes in the OC- |
| 10 | 192 signal, and |
| 11 | means for verifying correct operation of said encoding means and said |
| 12 | decoding means, The OC 192 input/output card of Claim 24 |
| 13 | wherein said encoding means and said decoding means use a |
| 14 | triple-error correcting Bose-Chaudhuri-Hocquenghem (BCH) |
| 15 | code. |
| 1 | 33. (Original) The OC-192 input/output card of Claim 25 wherein said |
| 2 | determining means includes an error accumulator located in said receiver, and means for |
| 3 | examining an error accumulator count of the error accumulator to match a number of |
| 4 | accumulated errors with the number of inserted errors. |
| 1 | 34. (Original) The OC-192 input/output card of Claim 30 wherein said tracking |
| 2 | means increments one or more registers in a location counter having at least first, second, |
| 3 | and third registers, the first register corresponding to a SONET column location, the |
| 4 | second register corresponding to an index location, and the third register corresponding to |
| 5 | a byte location, the index and byte locations together representing a SONET byte |
| 6 | location. |
| 1 | 35. (Original) The OC-192 input/output card of Claim 34 wherein said tracking |
| 2 | means contains 10 location counters, including: |
| 3 | a first location counter for tracking a location of a first error bit; |

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| 4 | second and third location counters nested together for tracking a location of a |
|---|---|
| 5 | second error bit; |
| 6 | fourth, fifth and sixth location counters nested together for tracking a location of a |
| 7 | third error bit; and |
| 8 | seventh, eighth and ninth location counters nested together for tracking a location |
| 9 | of a fourth error bit. |
| 1 | 36. (Original) The OC-192 input/output card of Claim 33 wherein said error |
| 2 | accumulator accumulates both corrected errors and uncorrectable errors. |
| 1 | 37. (Original) An error injection circuit comprising: |
| 2 | an error selection interface which programs a desired number of errors for |
| 3 | insertion into a plurality of data signals; |
| 4 | an encoding circuit which defines a plurality of code words of the data signals; |
| 5 | and |
| 6 | a location counter which increments through a plurality of locations in each of |
| 7 | the code words and inserts the desired number of errors into different ones |
| 8 | of the data signals at different code word permutation locations. |
| 1 | 38. (Original) The error injection circuit of Claim 37 wherein said location |
| 2 | counter means cycles through all possible permutations of all the code word locations. |
| 1 | 39. (Original) The error injection circuit of Claim 37 wherein: |
| 2 | the data signal is a SONET data signal having nine rows; and |
| 3 | said inserting means inserts errors in 32 code words defined within each of the |
| 4 | nine SONET rows. |
| 1 | 40. (Original) The error injection circuit of Claim 37 further comprising an error |
| 2 | mask which selectively prevents insertion of one or more of the errors in selected code |
| 3 | words |

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